Lecture No 12

Instruction set comparison

Instruction set comparison

- Instruction can be grouped into two classes

1) **F-type (Functional) instruction** that transforms data (ALU type operation) . These generally correspond one-to-one action specified by higher level language.
2) **M-type (Data movement) instruction** that position data for later use.(e.g. load or store). For many program these instruction are required by the instruction set not the source program.

M-Ratio:

- M ratio defines overall effectiveness of an architecture.
- M ratio is the ratio of data movement instruction to functional instruction.

$$\text{M-ratio} = \frac{\text{Number of M-type instructions}}{\text{Number of F-type instructions}}.$$

P- Ratio:

- P-type or procedural instruction is used to define those instruction that alter or modify instruction sequence.

$$\text{P-ratio} = \frac{\text{Number of P-type instructions}}{\text{Number of F-type instructions}}.$$

Cost-Area

- There are two types of cost

1)Fixed cost : The fixed cost includes the cost of engineering ,cost of both h/w & s/w, engineering charges to building VLSI masks, charges for both CAD equipment & s/w development & tooling manufacturing expense.

2)Marginal cost of manufacture : The marginal cost of manufacturer include cost to deliver .

- Area
- A processor designer has little control over fixed or variable cost. It is largely in the area of marginal manufacturing cost that design tradeoff is possible.
- All most all modern designs are based upon silicon technology in one or another VLSI formats. Given a set of VLSI technology There are two primary determinants of costs.

1. Pins(and package)
2. Silicon area occupied.

- Processor Area
- Most processor are implemented on one of few chips, each holding die about 10-15mm on a side. These die are produced in bulk from a larger wafer, perhaps 15-21cm in diameter.
- Defect normally occurs over the wafer surface(Figure 12).

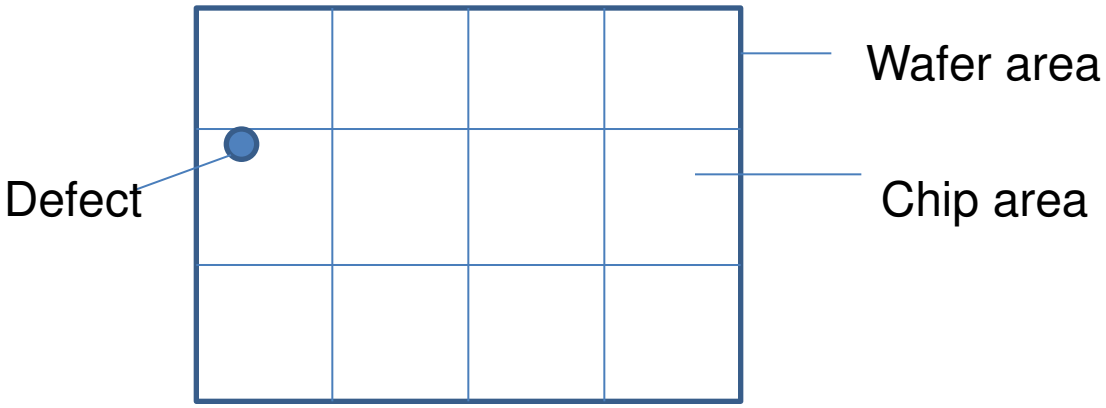

Figure 12. Defect distribution on wafer

- Large chip area require on absence of defects over that area.
- If chips are large for a particular processing technology, there will simply be no yield at all. Defects will be found on all the die a particular wafer.
- A good design is not necessarily one that immediately produces maximum yield.
- Reducing the area of a design below a certain critical amount has a marginal effects on yield, which at that point is simply determined by the percentage area affected by defects .Additionally small design waste area because there is a required seperation between adjacent die on a wafer, so small die size simply means a larger amount of area dedicated to interesting unused wafer area.
- Improvement in design process, largely due to photolithography allow large amount of processor logic to be included in a constant area.
- The area available to a designer is largely a function of the manufacturing processing technology .This includes the purity of the silicon crystals , the absence of dust & other impurities & the overall control of the diffusion & process technology.
- For the processor designer, there is a delicate design decision to be made early on what die area & what lithography ought we use to achieve a product with a maximum market impact.
- Suppose a die with a square aspect ratio area A about N of these die can be realized in a wafer of diameter d.(Figure 13).

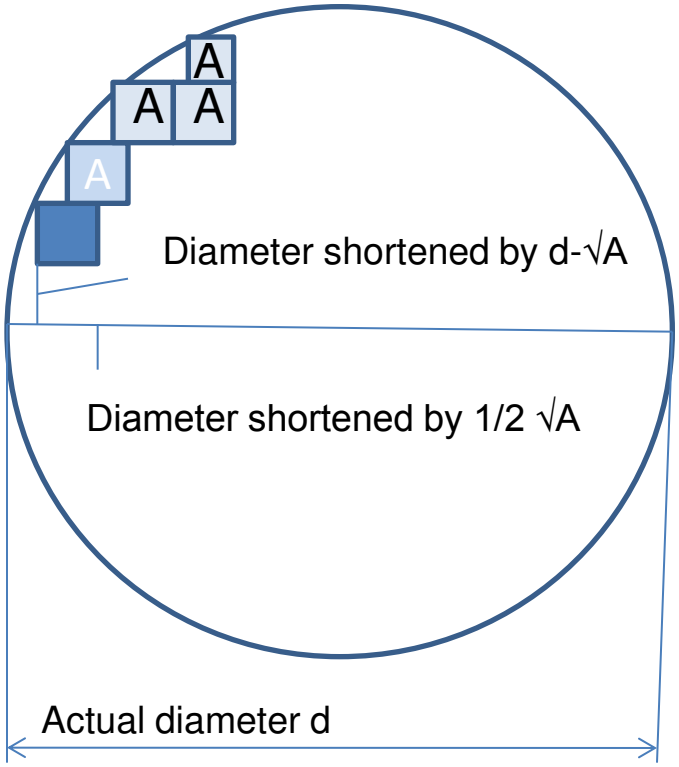

Figure . Number of die(of Area A) on a wafer of diameter d